

### Abstract of the Disclosure

5 A shift register device includes transistor  
pass gates and latches connected in series and disposed  
along a data bit line, each latch connected to a  
corresponding transistor pass gate. Each transistor pass  
gate is controlled by a separate control signal input  
line that provides a signal to the transistor pass gate  
connected to it. The signals are provided in a staggered  
10 time pattern beginning with a latch disposed last in  
succession, shifting data from one position to the next  
succeeding position. Each latch is capable of storing  
one bit of data. The shift register utilizes less  
silicon space while reducing the amount of power consumed  
15 during operation.